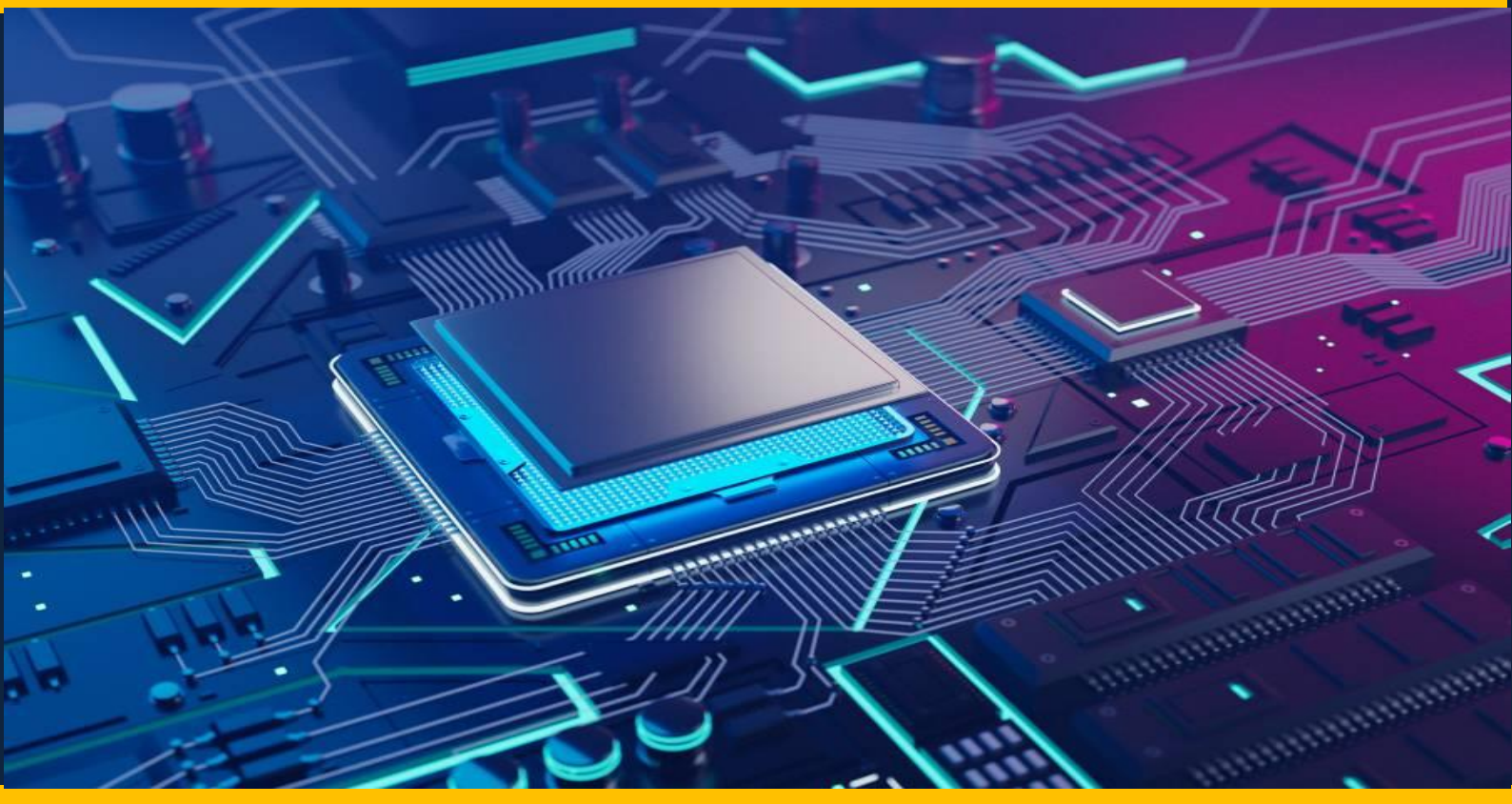
M.I.E.T. ENGINEERING COLLEGE
(Autonomous)

Curriculum & Syllabus

(Regulations 2024)



M.E. VLSI Design

M.I.E.T. ENGINEERING COLLEGE

(AUTONOMOUS)

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai)
Accredited by NBA (CIVIL, CSE, ECE, EEE & MECH)
Accredited with 'A+' grade by NAAC
(An ISO 9001:2015 Certified Institution)
(Recognized by UGC under section 2(f) & 12(B) of UGC Act, 1956)
TRICHY - PUDUKKOTTAI MAIN ROAD, TRICHY - 620 007

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CURRICULUM AND SYLLABUS

M.E. VLSI DESIGN

(Regulations 2024)

Vision

To be a top-class technical hub in imparting knowledge in cutting edge areas of Electronics and Communication Engineering, providing pleasant learning environment, nurturing scholars of excellent proficiency to meet the global and socio-economic challenges of the country.

Mission

- To provide remarkable teaching and research environment through state-of-the-art facilities.
- To strengthen the soft as well as hard skills of students to achieve technical and academic excellence.
- To raise the students to become responsible citizens with good human values and encourage them to work for the well-being of society.
- To develop the skills of lifelong learning and professional growth of students through utilization of the high-standard infrastructure facilities.

Program Outcomes (POs)

1. An ability to independently carry out research/investigation and developmentwork to solve practical problems
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
4. Understand the fundamentals involved in the Designing and Testing of electronic circuits in the VLSI domain.
5. Provide solutions through research to socially relevant issues for modern Electronic Design Automation (EDA) tools with knowledge, techniques, skills andfor the benefit of the society.
6. Interact effectively with the technical experts in industry and society.

Program Educational Objectives (PEO)

1. Graduates will be able to model, analyze, design, verify functionality, implement and test VLSI chips using relevant Electronic Design Automation Tool.
2. Graduates will be able to technically competent in design, development and implementation of electronics and VLSI design and extends into applications in the different thrust areas.
3. Graduates will be responsible member of society with ethics, eager to solve the real-world problem in VLSI technologies.

PO-PEO Mapping

Program Educational Objectives	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
PEO1	2	1	2	3	1	1
PEO2	3	1	2	3	2	2
PEO3	3	1	1	3	3	3

1 - Low, 2 - Medium, 3 – High

CHOICE BASED CREDIT SYSTEM

I TO IV SEMESTERS (REGULAR) CURRICULUM AND SYLLABUS

SEMESTER I

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
THEORY								
1.	24MA1101	Graph Theory and Optimization	FC	3	0	0	3	3
2.	24VL1101	Analog IC Design	PCC	3	0	0	3	3
3.	24VL1102	Digital CMOS VLSI Design	PCC	3	0	0	3	3
4.	24VL1103	Digital System Design using FPGA	PCC	3	0	0	3	3
5.	24VL1104	Semiconductor Devices and Modeling	PCC	3	0	0	3	3
6.	-	Professional Elective I	PEC	3	0	0	3	3
PRACTICAL								
7.	24VL1201	Digital System Design using FPGA Laboratory	PCC	0	0	4	4	2
8.	24VL1202	Analog IC Design Laboratory	PCC	0	0	4	4	2
							Total	**23**

SEMESTER II

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
THEORY								
1.	24VL2101	Design of ASICs	PCC	3	0	0	3	3
2.	24VL2103	RFIC Design	PCC	3	0	0	3	3
3.	24VL2104	VLSI Testing	PCC	3	0	0	3	3
4.	-	Professional Elective II	PEC	3	1	0	4	4
5.	-	Professional Elective III	PEC	3	1	0	4	4
6.	24RE2101	Scientific Report Writing	RMC	2	0	0	2	2
PRACTICAL								
7.	24VL2201	Design of ASIC using EDA tools	PCC	0	0	4	4	2
							Total	**21**

SEMESTER III

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
THEORY								
1.	24VL3101	VLSI Structures for Signal Processing	PCC	3	0	0	3	3
2.	-	Professional Elective IV	PEC	3	0	0	3	3
3.	-	Open Elective	OEC	3	0	0	3	3
4.	24RE3101	Research Methodology and IPR	RMC	2	0	0	2	2
PRACTICAL								
5.	24VL3501	Project Work Phase I	EEC	0	0	12	12	6
6.	24RE3201	Research Article Review	RMC	0	0	4	4	2
							Total	**19**

SEMESTER IV

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
PRACTICAL								
1.	24VL45s01	Project Work Phase II	EEC	0	0	24	24	12
							Total	**12**

TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE = 75

FOUNDATION COURSE (FC)

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
1.	24MA1101	Graph Theory and Optimization	FC	3	0	0	3	3
							Total	**3**

PROFESSIONAL CORE COURSES (PCC)

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
1.	24VL1101	Analog IC Design	PCC	3	0	0	3	3
2.	24VL1102	Digital CMOS VLSI Design	PCC	3	0	0	3	3
3.	24VL1103	Digital System Design using FPGA	PCC	3	0	0	3	3
4.	24VL1104	Semiconductor Devices and Modeling	PCC	3	0	0	3	3
5.	24VL1201	Digital System Design using FPGA Laboratory	PCC	0	0	4	4	2
6.	24VL1202	Analog IC Design Laboratory	PCC	0	0	4	4	2
7.	24VL2101	Design of ASICs	PCC	3	0	0	3	3
8.	24VL2103	RFIC Design	PCC	3	0	0	3	3
9.	24VL2104	VLSI Testing	PCC	3	0	0	3	3
10.	24VL2201	Design of ASICs using EDA Tools	PCC	0	0	4	4	2
11.	24VL3101	VLSI Structures for Signal Processing	PCC	3	0	0	3	3
							Total	**30**

PROFESSIONAL ELECTIVES COURSES (PEC)
SEMESTER II, PROFESSIONAL ELECTIVE I, II & III

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
1.	24VL2301	Opto Electronic Devices	PEC	3	1	0	4	4
2.	24VL2302	Electronic Design Automation using EDA Tools	PEC	3	1	0	4	4
3.	24VL2303	Electromagnetic Interference and Compatibility	PEC	3	1	0	4	4
4.	24VL2304	Data Converters	PEC	3	1	0	4	4
5.	24VL2305	Hardware Software Co-Design for FPGA	PEC	3	1	0	4	4
6.	24VL2306	Scripting Languages for Electronic Design Automation	PEC	3	1	0	4	4
7.	24VL2102	Low Power VLSI Design	PEC	3	1	0	4	4
8.	24VL3301	MEMS and NEMS	PEC	3	1	0	4	4

9.	24VL3302	Network on Chip	PEC	3	1	0	4	4
10.	24VL3303	Nanotechnology	PEC	3	1	0	4	4

SEMESTER III, PROFESSIONAL ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
1.	24PE1307	Energy Storage Systems	PEC	3	0	0	3	3
2.	24PE1308	Power Electronics for Renewable Energy Systems	PEC	3	0	0	3	3
3.	24PE1309	Advanced Power Converters	PEC	3	0	0	3	3
4.	24PE1310	Wind Energy Conversion System	PEC	3	0	0	3	3
5.	24PE1311	Grid Integration of Renewable Energy Sources	PEC	3	0	0	3	3
6.	24PE1312	Microcontroller Applications in Power Converters	PEC	3	0	0	3	3

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
1.	24RM1101	Research Methodology and IPR	RMC	2	0	0	2	2
2.	24RM2101	Scientific Report Writing	RMC	2	0	0	2	2
3.	24RM3201	Research Article Review	RMC	0	0	4	2	2

EMPLOYABILITY ENHANCEMENT COURSES (ECC)

S. NO.	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS PER WEEK	CREDITS
				L	T	P		
1.	24VL3201	Project Work Phase I	EEC	0	0	12	12	6
2.	24VL4201	Project Work Phase II	EEC	0	0	24	24	12

24MA1101 GRAPH THEORY AND OPTIMIZATION TECHNIQUES L T P C
3 0 0 3

COURSE OBJECTIVES

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real life situation.

UNIT I GRAPHS 9

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II GRAPH ALGORITHM 9

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III LINEAR PROGRAMMING 9

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT IV NON-LINEAR PROGRAMMING 9

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT V SIMULATION MODELLING 9

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

TOTAL : 45 PERIODS

COURSE OUTCOMES

On successful completion of this course, the student will be able to

CO1: Apply graph ideas is solving connectivity related problems.
CO2: Apply fundamental graph algorithms to solve certain optimization problems.
CO3: Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
CO4: Model various real life situations as optimization problems and effect their solution through Non-linear programming.
CO5: Apply simulation modeling techniques to problems drawn from industry management and other engineering fields.

TEXT BOOKS

1. Taha H.A, “Operation Research: An Introduction”, Ninth Edition, Pearson Education, New Delhi, 2010.
2. Gupta P. K, and Hira D.S., “Operation Research”, Revise Edition, S. Chand and Company Ltd., 2012.

3. Sharma J.K., "Operation Research", 3rd Edition, Macmillan Publishers India Ltd., 2009.

REFERENCE BOOKS

1. Douglas B. West, "Introduction to Graph Theory", Pearson Education, New Delhi, 2015.
2. 2. Balakrishna R., Ranganathan. K., " A text book of Graph Theory", Springer cience and Business Media, New Delhi, 2012.
3. 3. Narasingh Deo, "Graph Theory with Applications to Engineering and Computer Science",Prentice Hall India,1997.
4. 4. David avis "Graph Theory and Combinatorial Optimization", Springer-Verlag New York Inc,2010.
5. 5. Krishnaiyan KT, Thulasiraman, Subramanian Arumugam,"Handbook of Graph theory, Combinatorial Optimization", Chapman & Hall 2016.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	-
CO2	3	3	2	2	2	-
CO3	3	3	2	2	2	-
CO4	3	3	2	2	2	-
CO5	3	3	2	2	2	-
AVG	3	3	2	2	2	-

1 - Low, 2 - Medium, 3 – High, '-' No correlation

24VL1101 ANALOG IC DESIGN L T P C
3 0 0 3

COURSE OBJECTIVES

- To understand the basic principle of operation, the circuit choices and the trade offs involved in the MOS transistor level design
- To develop the ability to design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.
- To develop the skills to design analog VLSI circuits for a given specification

UNIT I CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS 9

MOS Device Models, MOS Current Sources and sinks, CS, CG and Source Follower, Differential amplifier-Single ended and differential operation, Cascode and Folded Cascode configurations.

UNIT II FREQUENCY RESPONSE AND NOISE CHARACTERISTICS OF AMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG, Source

Follower, Cascade and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op-Amps.

UNIT IV TWO STAGE OPAMPS AND FREQUENCY COMPENSATION 9

Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation.

UNIT V BAND GAP REFERENCES 9

Supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing. Case study-Design of Two stage opamp amplifiers to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures. Design of sub-µW bandgap circuits.

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Design current mirrors and amplifiers to meet user specifications
CO2: Analyse the frequency and noise performance of amplifiers
CO3: Design and analysis of feedback amplifiers and one stage op-amps
CO4: Design and analyse two stage op amps
CO5: Perform design and analysis of analog circuits for given specifications.

TEXT BOOKS

1. Behzad Razavi,"Design of Analog CMOS Integrated Circuits", TataMcgraw Hill, 2001.
2. Willey M.C.Sansen,"Analog Design Essentials",Springer,2006.
3. T.C.Carusone, D.A.Johns and K.W.Martin, "Analog Integrated Circuit Design," Second Edition, John WileyInc,2012.

REFERENCE BOOKS

1. Phillip E. Allen,Douglas R. Holberg,"CMOS Analog Circuit Design",OxfordUniversityPress,2nd,Edition,2002.
2. Paul. R. Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.
3. Jacob Baker, "CMOS: Circuit Design, Layout, And Simulation, Wiley IEEEPress,3rd ,Edition, 2010.
4. Behzad Razavi, "Design of Analog CMOS Integrated Circuits"MC Graw Hill Education,July 2015.
5. Carusone, David A. Johns, and Kenneth W. Martin, "ANalog Integrated Circuit Design",Wiley, 2013.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	2	2	-	-
CO2	1	-	2	2	-	-
CO3	1	-	2	2	-	-
CO4	1	-	2	2	-	-
CO5	1	-	2	2	-	-
AVG	1	-	2	2	-	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL1102 DIGITAL CMOS VLSI DESIGN L T P C
3 0 0 3

COURSE OBJECTIVES

- To lay rigorous foundation in basic CMOS digital circuits
- To build problem solving skills and creative circuit building capability
- To learn all important issues related to size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II STATIC AND DYNAMIC LOGIC CIRCUITS 9

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, dynamic logic gates design considerations, domino logic, interconnects.

UNIT III SEQUENTIAL CIRCUIT DESIGN AND TIMIMG ANALYSIS 9

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV MEMORIES 9

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read- Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers

UNIT V ARITHMETIC BUILDING BLOCK 9

Architectures for adders, accumulators, multipliers. Case study – Optimized design of adders, multipliers and barrels shifters for a given specification with special consideration to speed, power and area trade offs.

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Design CMOS inverter with optimized power, area and timing

CO2: Design optimized static and dynamic circuits using logical effort

CO3: Understand timing constraints in latches flip-flops and clocking issues

CO4: Design memories

CO5: Design low power digital VLSI circuits

TEXT BOOKS

1. N.Weste, K. Eshraghian, " Principles Of CMOS VLSI Design", Addision Wesley, 2nd Edition, 1993.
2. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits",Pearson,2016.
3. Perspective", Prentice Hall Of India, 2ndEdition, Feb2003. Samir Palnitkar, "Verilog HDL",SunSoft,1996.

REFERENCE BOOKS

1. T Pucknell and Eshraghian, "Basic VLSI Design", 3rd Edition, PHI, 1996.
2. Sung-MoKang & Yusuf Leblebici,"CMOS Digital Integrated Circuits Analysis and Design",Mcgraw-Hill,1998.
3. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective",3rd Edition, Pearson/Addison-Wesley, 2005.
4. Jan M. Rabaey,Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits", 2nd Edition, Pearson/Addison-Wesley,2003.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	2	2	-	-
CO2	1	-	2	2	-	-
CO3	1	-	2	2	-	-
CO4	1	-	2	2	-	-
CO5	1	-	2	2	-	-
AVG	1	-	2	3	-	-

1-Low, 2-Medium, 3-High, '-'-No correlation

24VL1103 DIGITAL SYSTEM DESIGN USING FPGA L T P C

3 0 0 3

COURSE OBJECTIVES

- Understand the various abstraction level in Verilog HDL and model the complex combinational and sequential circuits with Verilog HDL
- Provide in depth understanding of state machine design and modeling using Verilog HDL
- Understand about different FPGA Architecture like Xilinx and ALTERA

UNIT I VERILOG HDL-STRUCTURAL AND BEHAVIORAL MODELING 9

Verilog Fundamentals-Operators-Gate Level Modeling -Data Flow Modeling-Test Bench-Behavioral Level Modeling -Procedural Assignment Statements-Blocking and Non Blocking Assignments-Tasks & Functions-System Tasks & Compiler Directives.

UNIT II DESIGN AND MODELING OF COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Ripple Carry Adders-Carry Look Ahead Adder- Unsigned Binary Multipliers.Synthesizable Coding Style for Combinational Circuits.FSM modeling of sequence detector-Serial adder-Vending machine. Synthesizable coding style for sequential circuits and FSM.

UNIT III MEMORY AND SYSTEM DESIGN 9

Synchrronous and Asychronous FIFO -Single port and Dual Port ROM and RAM. Traffic Light Controller, Real Time clock-Interfacing using FPGA:VGA,LCD,CAMERAS.

UNIT IV FPGA ARCHITECTURE 9

Types of programmable logic devices: PLA,PAL,CPLD-FPGA Architecture -Programming Technologies-Chip I/O Programmable Logic Blocks-Fabric and Architecture of FPGA-Xilinx/Intel/Actel FPGA Architecture.

UNIT V SOC ARCHITECTURE 9

An overview of System on Design -FPGA SoC Architecture Case Study:

1. Binary counter-Bus protocol
2. Xilinx/Intel FPGA

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Analyse and design synchronous sequential circuits.

CO2: Analyse hazards and design asynchronous sequential circuits.

CO3: Knowledge on the testing procedure for combinational circuit and PLA.

CO4: Able to design PLD and ROM.

CO5: Design and use programming tools for implementing digital circuits of industry.

TEXT BOOKS

1. Michael D Ciletti, Advanced Digital Design with the Verilog HDL,2017,Second Edition, Pearson Education.
2. Ming Bo Lin,Digital System Design and Practice:Using Verilog HDL andFPGAs,2015,Second Edition,Create Space Independent Publishing Platform.
3. Wayne Wolf, FPGA Based System Design, 2011,Prentices Hall Modern Semiconductor Design Series.

REFERENCE BOOKS

1. Charles H Roth Jr,Lizy Kurian John and Byeong Kil Lee,Digital Dystems Design using Verilog, 2016,First Edition,Cengage Learning.

2. Joseph Yu,System-on-Chip,Design with Arm Cortex-M Processors,2019,ARM Education Media.
3. By Cem Unsalan, Bora Tar, "Digital System Design with FPGA: Implementation Using Verilog and VHDL",MC Graw Hill,2017.
4. Ross K. Snider, "Advanced Digital System Design using SoC FPGAs",Springer,2023.
5. Ian Grout, "Digital Systems Design with FPGAs and CPLDs",Elsevier,2008.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	1	1	1	-
CO2	1	-	1	1	1	-
CO3	1	-	1	1	1	-
CO4	1	-	1	1	2	-
CO5	1	-	1	1	1	-
AVG	1	-	1	1	1.2	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL1104 SEMICONDUCTOR DEVICES AND MODELING L T P C
3 0 0 3

COURSE OBJECTIVES

- To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.
- To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications
- To acquire the fundamental knowledge of different semiconductor device modelling aspects.

UNIT I BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time.

UNIT II MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche

Breakdown, Band-to-Band Tunneling, Injection of Hot Carriers from Silicon into Silicon Dioxide.

UNIT III MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields.

UNIT IV CMOS DEVICE DESIGN 9

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT V MOSFET ADVANCED TECHNOLOGIES 9

Combinational Circuits. Interconnects – Electro static discharge (ESD) – Latch-up and its Prevention ,MOSFET structure evolution – High-k dielectrics,Metal Gate Electrodes, High mobility substrates (Strained Si, Ge), Elevated S/D.

Case study:

1. Reliability Analysis of High-k Dielectrics in MOSFETs
2. Design and Optimization of ESD Protection Circuits

TOTAL: 45 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Discuss the device level characteristics of BJT transistors.
CO2: Explore the properties of MOS capacitors.
CO3: Analyze the various characteristics of MOSFET devices.
CO4: Describe the various CMOS design parameters and their impact on performance.
CO5: Ability to analyse the transistor level circuits.

TEXT BOOKS

1. Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.
2. A.B. Bhattacharyya “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Ltd, 2009.
3. Ansgar Jungel, “Transport Equations for Semiconductors”, Springer, 2009.

REFERENCE BOOKS

1. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition,2014.

2. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis and Design, Third Edition, Tata McGraw-Hill, 2003.
3. Neil H. E. Weste and David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Edition, Addison Wesley, 2010.
4. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2004.
5. Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 1984.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	2	-	-
CO2	3	-	2	2	-	-
CO3	2	-	2	2	-	-
CO4	2	-	2	2	-	-
CO5	2	-	2	2	2	-
AVG	2	-	2	2	2	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL1201 DIGITAL SYSTEM DESIGN USING FPGA LABORATORY L T P C
0 0 4 2

COURSE OBJECTIVES

- To help engineers read, understand, and maintain digital hardware models.
- To form strong foundation on conventional verification test benches written in Verilog and System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog.

LIST OF EXPERIMENTS

1. Adder/ Subtractor and Multiplexer/ Demultiplexer
2. Encoder/ Priority Encoder
3. Code Converter ,Comparator
4. Flip flop-Shift Register/ Universal Shift Register
5. Up counter/ Down counter
6. Design of 8-bit Carry Skip Adder and Carry Save Adder
7. Design of 4-bit Array Multiplier with and without Pipelining
8. Design of 4-tap FIR Filter with and without Pipelining
9. Design of FIFO
10. Design of Sequence Detector
11. Design of 8-bit ALU

12. Study of FPGA

TOTAL: 60 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: To learn the basic HDL functions.

CO2: Design and analyse the combinational and sequential circuits using Verilog HDL tools.

CO3: Perform FPGA Implementation for Verilog HDL designs on development.

CO4: Implement FIR algorithms in FPGA.

CO5: Implement ALU in FPGA.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	1	1	1
CO2	1	1	1	1	1	1
CO3	1	1	1	1	1	1
CO4	1	1	1	1	1	1
CO5	1	1	1	1	1	1
AVG	1	1	1	1	1	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL1202 ANALOG IC DESIGN LABORATORY **L T P C**
0 0 4 2

COURSE OBJECTIVES

- Analyze and design single ended and differential IC amplifiers.
- Understand the relationships between devices, circuits and systems
- Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs

LIST OF EXPERIMENTS

1. Simulation of MOSFET IV characteristics, second order parameters.
2. Simulation of CMOS inverter-DC,AC.
3. Simulation of Transient Analysis.
4. Post layout simulation.
5. Design of basic single stage amplifiers(Common Source,Common Gate and Common Drain)
6. Analysis and Design of Simple current mirror and cascode current mirror.
7. Analysis and Design of differential amplifier with active load and current source load.
8. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

9. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter.
10. Analysis and Design of Two-Stage Opamp with Frequency Compensation.
11. To study layouts of CMOS combinational and sequential circuits.
12. To utilize switch-level and circuit-level simulators for the logic verification and timing simulation.

TOTAL: 60 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: Introduce industry standard Analog IC design EDA tool

CO2: Practical learning and understanding of Analog amplifiers, current mirrors etc.

CO3: Solve analog design problems by changing the design parameter of the circuit with the help of LTSpice.

CO4: Understand the working of oscillators and differential circuits.

CO5: Learn the art of designing power efficient opamps

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	1	1	1
CO2	1	1	1	1	1	1
CO3	1	1	1	1	1	1
CO4	1	1	1	1	1	1
CO5	1	1	1	1	1	1
AVG	1	1	1	1	1	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL2101 DESIGN OF ASICS L T P C
3 0 0 3

COURSE OBJECTIVES

- To deal with the entire FPGA and ASIC Design Flow from the Circuit and Layout Design Point of View.
- To give the student an understanding of basics of System on Chip design.
- To understand case study of Finite State Machine.

UNIT I ASIC DESIGN METHODOLOGY AND DESIGN FLOW 9

Implementation strategies for digital ICs: Custom IC Design – Cell-based Design Methodology – Array based Implementation Approaches-Traditional and Physical Compiler based ASIC Flow.

UNIT II RTL SYNTHESIS 9

RTL Synthesis Flow – Synthesis Design Environment and Constraints – Architecture of

Logic Synthesizer – Technology Library Basics – Components of Technology Library – Synthesis Optimization – Technology independent and dependent Synthesis – Data path Synthesis – Low power Synthesis.

UNIT III LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.

UNIT IV SYSTEM ON CHIP DESIGN 9

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators.

UNIT V CASE STUDY- FSM 9

Case study: FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs (I2C, PWM, GPIO, SPI, NAND, Ethernet, USB, high speed serdes etc. are interconnected through AXI/APB buses (protocols and interconnects)

TOTAL: 45 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: Understand methodology and Design flow in ASICs.
CO2: Describe the issues involved in ASIC design.
CO3: Analyse to use Algorithms for Floor Planning and Placement of Cells.
CO4: Understand to analyse High Performance Algorithms.
CO5: Analyse to Finite State Machines.

TEXT BOOKS

1. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999.
2. M.J.S Smith, “Application Specific Integrated Circuits”, Pearson, 2003.
3. Jan.M.Rabaey et al, “Digital Integrated Circuit Design Perspective”, 2nd Edition, PHI 2003.

REFERENCE BOOKS

1. Hoi-Jun Yoo, Kangmin Lee and Jun Kyong Kim, “Low-Power NoC for High-Performance SoC Design”, CRC Press, 2008.
2. An Integrated Formal Verification solution DSM sign-off market trends”, www.cadence.com.
3. David A.Hodges, “Analysis and Design of Digital Integrated Circuits”, 3rd Edition, MGH 2004.
4. Khosrow Golshan, “Physical Design Essentials”, Springer,2007.
5. Keith Barr, “ASIC Design in the Silicon Sandbox: A Complete Guide to Building Mixed-Signal Integrated Circuits”,McGraw-Hill,2006.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	2	1
CO2	2	1	1	2	2	1
CO3	2	1	1	2	2	1
CO4	2	1	1	2	2	1
CO5	2	1	1	2	2	1
AVG	2	1	1	2	2	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL2103 RFIC DESIGN L T P C
3 0 0 3

COURSE OBJECTIVES

- Understand the Concept of RFIC Design.
- Understand the High Frequency Model of MOS and importance of Impendence Matching.
- Understand functional Design Aspects of Mixers, PLL, analyze and design of Transceivers.

UNIT I INTRODUCTION TO WIRELESS AND RF TECHNOLOGY 9

Complexity design and Applications – Choice of Technology – basic Concepts in RF Design: Non Linearity – Time Variance – Intersymbol Interference - Random Processes – Noise. Definitions of Sensitivity – dynamic range- Conversion gain and Distortion.

UNIT II HIGH FREQUENCY MODEL OF RF TRANSISTORS AND MATCHING NETWORKS 9

MOSFET behavior at RF Frequencies – Noise Performance and limitation of devices – Impedance matching networks – transformers and baluns.

UNIT III ACTIVE AND PASSIVE MIXERS 9

Qualitative Description of the Gilbert Mixer - Conversion Gain, and Distortion and Noise , Analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - a Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV PLL AND FREQUENCY SYNTHESIZERS 9

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency

Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer.

UNIT V DESIGN OF TRANSCEIVER 9

Case study: System level specification and design of Receiver , Transmitter and Frequency Synthesizer

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: Understand the concept of RFIC Design.

CO2: Understand the High Frequency Model of MOS and Importance of Impedance Matching.

CO3: To analyze and design mixers.

CO4: Design PLL and frequency synthesizer.

CO5: Analyze and Design of Transceivers.

TEXT BOOKS

1. Hooman Darabi, "Radio Frequency Integrated Circuits and Systems", 2020, 2nd Edition, Cambridge University Press, NewYork, USA.
2. B Razavi, "RF Microelectronics", Prentice Hall, 1998.
3. Richard Chi-Hsi Li, "RF Circuit Design, 2nd Edition", Wiley,2012.

REFERENCE BOOKS

1. Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001.
2. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press, 2003.
3. Richard C. Li , "RF Circuit Design", Wiley,2008.
4. John W. M. Rogers, Calvin Plett, "Radio Frequency Integrated Circuit Design",Pearson 2003.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mcgraw-Hill, 1999.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	2	1
CO2	2	1	1	2	2	1
CO3	2	1	1	2	2	1
CO4	2	1	1	2	2	1
CO5	2	1	1	2	2	1
AVG	2	1	1	2	2	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL2104 VLSI TESTING L T P C
3 0 0 3

COURSE OBJECTIVES

- To introduce the concept of VLSI testing.
- To introduce logic and fault simulation and testability measures
- To study the test generation for combinational and sequential circuits

UNIT I INTRODUCTION TO VLSI TESTING 9

Testing of VLSI Circuits– Fault Modeling – Equivalence and Dominance - Logic and Fault Simulation –Testability Measures – Combinational Circuit Test Generation – Redundancy Identification.

UNIT II LOGIC & FAULT SIMULATION & TESTABILITY MEASURES 9

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Testable Combinational Logic Circuit Design – Design of Testable Sequential Circuits– BIST Architectures –Random Logic Bist –Test-Per-Clock – Test-Per-Scan - BIST Systems – Memory BIST –At-speed Testing– Boundary Scan Architecture – JTAG Standards.

UNIT IV DESIGN FOR TESTABILITY 9

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture –DFT for Other Test Objectives

UNIT V CASE STUDY ON TESTING 9

Combinational Logic Circuit Design- Sequential Circuits design-Real time application

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: Identify the various IC fabrication methods.
CO2: Express the Layout of simple MOS circuit using true value and fault simulation.
CO3: Apply the BIST Architectures design rules for subsystem design.
CO4: Differentiate various FPGA,scan architectures
CO5: Design an real time application using VLSI testing.

TEXT BOOKS

1. M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005.
2. H. Fujiwara, Logic Testing and Design for Testability, MIT Press, 1985.
3. M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, IEEE Press, 1994.

REFERENCE BOOKS

1. M. Huth and M. Ryan, Logic in Computer Science, Cambridge Univ. Press, 2004
2. T. Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000.
3. D. Baik, K. K. Saluja and S. Kajihara, `Random Access Scan: a solution to test power, test data volume and test time`, International Conference on VLSI Design, Jan. 2004
4. H. Fujiwara, `A new class of sequential circuits with combinational test generation complexity`, IEEE Trans. on Computers, Vol. 49, No. 5, Sep 2000, pp. 895-905
5. S. Ohtake, T. Masuzawa, and H. Fujiwara, `A non-scan DfT method for controllers to achieve complete fault efficiency`, Proc. of the IEEE Asian Test Symposium (ATS) 1998, pp. 204-211.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	2	1	1
CO2	1	1	1	2	1	1
CO3	1	1	1	2	1	1
CO4	1	1	1	2	1	1
CO5	2	2	1	1	2	2
AVG	1	1	1	2	1	1

1-Low, 2-Medium, 3-High, '-'- No Correlation

24RE2101 SCIENTIFIC REPORT WRITING L T P C
2 0 0 2

COURSE OBJECTIVES

- To teach the basic paper writing process and learn how to collect relevant bibliography
- To summarize the skills needed to study all the bibliography
- To infer the skills needed when writing the title,abstract, conclusion etc. and prepare for quality paper at very first-time submission

UNIT I INTRODUCTION TO SUBJECT SELECTION 9

Selecting a subject-narrowing the subject into a topic - Stating an objective

UNIT II PREPARATION FOR PAPER WRITING 9

Preparing a working outline- Collecting the relevant bibliography (atleast 15 journal papers)

UNIT III LINKING OF PAPERS 9

Studying the papers - understanding the authors contributions - analysing each paper- Linking the papers

UNIT IV INTRODUCTION TO WRITING SKILLS **9**

Key skills are needed when writing a Title- key skills are needed when writing an Abstract- key skills are needed when writing an Introduction- Preparing conclusions based on the reading of all the papers.

UNIT V WRITING THE FINAL PAPER **9**

Writing the Final Paper -checking Plagiarism –case study: draft paper preparation- conference submission(national level)-journal publication

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: Understand the basic paper writing skills .

CO2: Learn how to collect relevant papers and preparing the working outline.

CO3: Understand the skills needed when studying the relevant papers

CO4: Understand the skills needed when writing the paper

CO5: Ensure the good quality of paper at very first-time submission

TEXT BOOKS

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006.
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006.

REFERENCE BOOKS

1. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.
2. Sheela P. Turbek, Taylor M. Chock,Lauren G. Shoemaker, Lara Vimercati, "Scientific Writing Made Easy: A Step-by-Step Guide to Undergraduate Writing in the Biological Sciences",Bullet IN 2006.
3. Rafal Marszalek, "Scientific Reports", Nature Portfolio,2011.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	1	1	1
CO2	1	1	1	1	1	1
CO3	1	1	1	1	1	1
CO4	1	1	1	1	1	1
CO5	1	1	1	1	1	2
AVG	1	1	1	1	1	1

1-Low, 2-Medium, 3-High, '-'- No Correlation

24VL2201 DESIGN OF ASICS USING EDA TOOLS L T P C
0 0 4 2

COURSE OBJECTIVES

- To help engineers read, understand, and simulate digital hardware models
- To perform conventional verification of test benches written in Verilog and System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog.

LIST OF EXPERIMENTS

1. Adder/ Subtractor and Multiplexer/ Demultiplexer
2. Encoder/ Priority Encoder
3. Code Converter, Comparator
4. Flip flop-Shift Register/ Universal Shift Register
5. Up counter/ Down counter
6. Design of 8-bit Carry Skip Adder and Carry Save Adder
7. Design of 4-bit Array Multiplier with and without Pipelining
8. Design of 4-tap FIR Filter with and without Pipelining
9. Design of FIFO
10. Design of Sequence Detector
11. Design of 8-bit ALU
12. Design of MAC unit using Verilog.

TOTAL: 60 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: Familiarize with sophisticated VLSI CAD tools available in the lab.
CO2: Able to design and implement any ASIC designs using the latest VLSI CAD tools.
CO3: Perform full custom ASIC design of digital blocks
CO4: Learn advanced features in physical design
CO5: Perform a complete cycle of chip design from design to chip tape-out procedure

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	2	1
CO2	2	1	1	2	2	1
CO3	2	1	1	2	2	1
CO4	2	1	1	2	2	1
CO5	2	1	1	2	2	1
AVG	2	1	1	2	2	1

1-Low, 2-Medium, 3-High, '-'- No Correlation

24VL3101 VLSI STRUCTURES FOR SIGNAL PROCESSING L T P C
3 0 0 3

COURSE OBJECTIVES

- To introduce techniques for altering existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI.
- To enhance the knowledge on the concepts of pipelining and bit level architecture.

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – typical DSP algorithms, data flow and dependence graphs – critical path, loop bound, iteration bound, longest path matrix algorithm, pipelining and parallel processing of FIR filters, pipelining and parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, algorithmic strengthreduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture,rank-order filters, Odd-Even, Merge-Sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, design of lyon's bit-serial multipliers using Horner's rule,

bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS AND ASYNCHRONOUS PIPELINING **9**

Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining - Bundled Dataversus Dual-Rail protocol.

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Determine the parameters influencing the efficiency of DSP architectures.
CO2: Analyse and modify the design equations leading to efficient DSP architectures.
CO3: Speed up convolution process and develop fast and area efficient IIR structures.
CO4: Develop fast and area efficient multiplier architectures.
CO5: Analyse to reduce multiplications and build fast hardware for synchronous digital systems

TEXT BOOKS

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation ", Wiley, Interscience, 2007.
2. Magdy A. Bayoumi, Earl E. Swartzlander, "VLSI Signal Processing Technology", Springer,1994.
3. J. D. Plummer, M. D. Deal and P. B. Griffin, Silicon VLSI Technology Fundamentals, Practice and Models, Prentice Hall, 2000

REFERENCE BOOKS

1. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.
2. J.G. Proakis and D.G. Manolakis, Digital Signal Processing, Third Edition, Prentice Hall,2007.
3. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.
4. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
5. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singal processing, Prentice Hall, 1985.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	2	2	1	-
CO2	1	-	2	2	1	-
CO3	1	-	2	2	1	-
CO4	1	-	2	2	1	-
CO5	1	-	2	2	1	-
AVG	1	-	2	2	1	-

1-Low, 2-Medium, 3-High, '-'- No Correlation

24RE3101 RESEARCH METHODOLOGY AND IPR L T P C
2 0 0 2

COURSE OBJECTIVES

- To arrange the conditions for collection and analysis of data in a manner that aims to combine relevance to the research purpose and ensure accuracy
- To transform and model the collected data to discover useful information for decision- making
- To create public awareness about the benefits of Intellectual property among students and provide legal certainty to inventors/ Patent applicants

UNIT I RESEARCH DESIGN **6**

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES **6**

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods.Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING **6**

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS **6**

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V PATENTS **6**

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL:30 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Ability to arrange the conditions for collection and analysis of data in a manner that aims to combine relevance to the research purpose.

CO2: Ability to gather information in a measured and systematic manner to ensure accuracy and data analysis.

CO3: Ability to transform and model the collected data to discover useful information for decision- making.

CO4: Ability to awareness about the benefits of Intellectual property.

CO5: Ability to take up legal certainty while applying for Patent.

TEXT BOOKS

1. Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.
3. K R N Aswini, "Research Methodology & Intellectual Property Rights", Pearson 2024.

REFERENCE BOOKS

1. David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
2. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.
3. C.R.Kothari, "Research Methodology Methods and Techniques", New age international publishers,1990.
4. Dr. Santosh M Nejakar, Dr. Harish Bendigeri "Research Methodology and Intellectual Property Rights", ISBN 978-93-5987-928-4, Edition: 2023-24.
5. N.K.Acharya, "Intellectual Property Rights", Asia Law House 6th Edition. ISBN: 978-93-81849-30-9,2023.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	-	-	2	-
CO2	3	3	-	-	1	-
CO3	2	3	-	-	1	-
CO4	1	1	-	-	3	-
CO5	1	1	-	-	3	-
AVG	**2**	**2**	-	-	**2**	-

1-Low, 2-Medium, 3-High, '-'- No Correlation

24RE3201 RESEARCH ARTICLE REVIEW L T P C
0 0 4 2

COURSE OBJECTIVES

- Thorough review of an article
- Proper planning and preparation of draft
- Write a proper review of the article

STAGES OF REVIEW

Stage-1	Collection of latest Research articles
Stage-2	Read the entire article and take a note in his/her own words.
Stage-3	Summarize the literature in his/her own words.
Stage-4	Classify and arrange the literatures with template
Stage-5	Preparation of review article
Stage-6	Plagiarism checked by the department and it must be less than 10%
Stage-7	Article must be communicated to the journal.

The students must do the above work individually by the guidance of faculty members and one coordinator is required to monitor the work progress. The evaluation will be done based on the following

a) Review of work after stage 3 10%
b) Review of work after stage 5 20%
c) Review of work after stage 7 20%
d) Final examination 50%

TOTAL: 60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Understand the technique to collect the literatures from various resources.
CO2: Apply the knowledge for collecting the required research data from the articles

CO3: Formulate the research problem.
CO4: Analyze the research gap from various researchers work.
CO5: Create the new article to publish in the research journals.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	1	1	1
CO2	1	1	1	1	1	1
CO3	1	1	1	1	1	1
CO4	1	1	1	1	1	1
CO5	1	1	1	1	1	1
AVG	1	1	1	1	1	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL3501 PROJECT WORK PHASE I L T P C
0 0 12 6

COURSE OBJECTIVES

- To develop knowledge to formulate a real-world problem.
- To use different tools and techniques to arrive at a solution.
- To prepare a report and give a presentation.

Project Guidelines and Evaluation

- **Selection of a project topic:** It is a crucial and involves a literature survey and creative input, guided by a project supervisor. The topic should allow skill development in design, fabrication, analysis, testing, and research.
- **Literature survey**: Which helps to identify gaps and build on existing research. Initial project work should be completed during Dissertation I to lay the groundwork for further research.
- **Completed project work phase-I:** will be evaluated by internal and external examiners based on an oral presentation and the project report, which is submitted at the end of Dissertation-I. The evaluation follows the institution's credit system regulations.

ESSENTIALS

1. **ZEROTH REVIEW:** Confirmed project title, Print out of base paper, abstract, with minimum of **6 slides** of Power Point Presentation.

2. **FIRST REVIEW:** Reply for queries (if any) given in **ZEROTH REVIEW**, clear idea about existing and collection of clear literature survey (Minimum of 20 articles)

from the reputed journals, with minimum of 15 slides. 25% of work should be completed.

3. **SECOND REVIEW:** Reply for queries (if any) given in **FIRST REVIEW,** collect and prepare the literatures (Minimum of 50 articles) with Literature template, minimum of **30 slides. 50%** of work should be completed.

4. **THIRD REVIEW:** Reply for queries (if any) given in **SECOND REVIEW, 90%** of work completion including Research Gap, Problem statement, Project Workflow Chart, Study of proposed work comparing with existing literatures Example: Calculation, Simulations, Analysis, optimization with minimum of **45 slides.**

TOTAL:180 PERIODS

COURSE OUTCOMES

On successful completion of this course, the student will be able to

CO1: Design and analyze, an identified problem using scientific tools.
CO2: Simulation/ Theoretical analysis of a physical system.
CO3: Integrate various domain knowledge for a sustainable solution.
CO4: Set Goals, Targets, timeline, plan and execute activities of the project.
CO5: Disseminate work both in oral and written format.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	-	-	-
CO2	2	3	2	-	-	-
CO3	3	3	3	-	-	-
CO4	3	3	2	-	-	-
CO5	2	3	3	-	-	-
AVG	3	3	2	-	-	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL4501 PROJECT WORK PHASE II L T P C
0 0 24 12

COURSE OBJECTIVES

- To define the problem of the proposed research work.
- To enable students to apply any piece of theory and experiments which they have learned to a specific problem related to industry / research.
- To demonstrate and validate the results of the design concept.

ESSENTIALS

1. ZEROTH REVIEW: Confirmed project title, Print out of base paper, abstract, with minimum of **6 slides** of Power Point Presentation.

2.FIRST REVIEW: Reply for queries (if any) given in **ZEROTH REVIEW**, clear idea about existing and proposed project work, clear literature survey, with minimum of **15 slides**.

3. SECOND REVIEW: Reply for queries (if any) given in **FIRST REVIEW,** nearly **30%** of work completion including Project Workflow Chart, Design, Calculation with minimum of **20 slides.**

4. THIRD REVIEW: Reply for queries (if any) given in **SECOND REVIEW, 50%** of work completion including Project Workflow Chart, Design, Calculation, simulations, Fabrication, with minimum of **25 slides.**

TOTAL: 360 PERIODS

COURSE OUTCOMES

On successful completion of this course, the student will be able to

CO1: Identify and formulate research problem.
CO2: Design and develop solution to the problem.
CO3: Analyze and solve the complex problems.
CO4: Plan, implement and execute the project.
CO5: Write effective technical report and demonstrate through presentation.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	3	-	-
CO2	2	2	3	3	-	-
CO3	2	2	3	3	-	-
CO4	2	2	3	3	-	-
CO5	2	2	3	3	-	-
AVG	2	2	3	3	-	-

1-Low, 2-Medium, 3-High, '-' - No correlation

24VL2301 OPTOELECTRONIC DEVICES L T P C
3 1 0 4

COURSE OBJECTIVES

- To study the basics concepts of optical system, optoelectronic devices and materials
- To learn the fundamental concepts in Semiconducting materials
- To design the integrated optical active and passive components

UNIT I INTRODUCTION TO OPTICAL SYSTEMS **12**

Introduction: Optical Systems and Fundamentals - Basics of Semi-conductor Optics: Elemental and Compound Semiconductors - Electronic and Optical Processes in Semiconductors; P-N Junctions LEDs, Photodetectors and Solar Cells.

UNIT II BASIC OPTOELECTRONIC DEVICES **12**

Optoelectronic devices: light detectors and solar cells – light emitting diode – laser diode - optical processes in organic semiconductor devices –excitonic state–Electro-optics and nonlinear optics: Modulators and switching devices – plasmonics

UNIT III OPTICAL PROCESSES IN SEMICONDUCTORS **12**

Classification of optical materials – Optical processes in semiconductors: optical absorption and emission, charge injection and recombination, optical absorption, loss and gain. Optical processes in quantum wells.

UNIT IV OPTICAL AND OPTOELECTRONIC MATERIALS **12**

Principles of photoconductivity - effect of impurities - principles of luminescence-laser principles - He-Ne, injection lasers, LED materials - binary, ternary photoelectronic materials - LCD materials - photo detectors - applications of optoelectronic materials - optical fibres and materials - electro optic modulators - Kerr effect - Pockels effect.

UNIT V OPTICAL PASSIVE AND ACTIVE COMPONENTS **12**

Integrated Optical Passive and Active Components: Case Study on Tunable Filters, Delay-Lines and Switching Circuits in SOI Platform

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Understand the basics concepts of optical system
CO2: Describe the different optoelectronic devices
CO3: Understand the fundamental concepts in Semiconducting materials
CO4: Understand the different optoelectronic materials used
CO5: Design the integrated optical active and passive components

TOTAL: 60 PERIODS

TEXT BOOKS

1. C. Kittel, “Introduction to Solid State Physics”, 7th Edition, John Wiley & Sons,Singapore, (2006).
2. Jasprit Singh, “Semiconductor Optoelectronics: Physics and Technology”, McGraw-Hill Education (Indian Edition), 2019.
3. S.C.Gupta, “Optoelectronic Devices and Systems”, Second Edition,2015.

REFERENCE BOOKS

1. Mark Fox, “Optical Properties of Solids”, Oxford Univ.Press, 2001.
2. Pallab Bhattacharya, “Semiconductor Optoelectronic Devices”, Pearson Education,2017.
3. B. Saleh, New York, “Fundamentals of Photonics”, Wiley,1991.
4. R. A. Smith, “Semiconductors”, Cambridge, University Press, 1978.

5. E. Rosencher & B. Vinter, “Optoelectronics”, Cambridge, University Press,2002.

Mapping of COs and POs

COs	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	1	1	-	-
CO2	1	-	1	1	-	-
CO3	2	-	1	1	-	-
CO4	2	-	1	1	-	-
CO5	1	-	1	1	-	-
AVG	**2**	**-**	**1**	**1**	**-**	**-**

1-Low, 2-Medium, 3-High, ‘-’- No correlation

24VL2302 ELECTRONIC DESIGN AUTOMATION TOOLS L T P C
3 1 0 4

COURSE OBJECTIVES

- To extend the knowldege on PSpice code for electronics circuits
- To learn synthesize Verilog and VHDL code and design circuits using verilog
- To apply the concept of designing and testing in real world scenario.

UNIT I INTRODUCTION TO SCRIPTING LANGUAGE 12

OS Architecture: System settings and configuration- Introduction to UNIX commands - Handling directories- Filters and Piping- Wildcards -Regular expression- Power Filters - Files Redirection. Working on Vi editor- Basic Shell Programming-TCL Scripting language.

UNIT II DESIGN AND ANALYSIS OF CIRCUITS USING SPICE 12

Circuit simulation using Spice - circuit description. AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and Opamp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits.

UNIT III SYNTHESIS AND SIMULATION USING HDLS 12

Synthesis and simulation using HDLs-Logic synthesis using Verilog. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

UNIT IV INTRODUCTION TO VERILOG 12

System Verilog- Introduction, Design hierarchy, Data types, Operators and language constructs. Functional coverage, Assertions, Interfaces and test bench structures.

Analog/Mixed Signal Modelling and Verification: Analog/Mixed signal modelling using Verilog-A and Verilog-AMS.

UNIT V CASE STUDY USING EDA TOOLS **12**

Designing a High-Speed ADC with EDA Tools, Designing a System-on-Chip (SoC) for a Mobile Device

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Write the scripting language for circuit design using EDA tool.
CO2: Write PSpice code for any electronics circuit and to perform monte-carlo analysis and sensitivity/worst case analysis
CO3: Design synthesizable Verilog and VHDL code.
CO4: Analyze the designing of circuits using verilog.
CO5: Design and test in real world scenario using EDA tools.

TOTAL:60 PERIODS

TEXT BOOKS

1. H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.
2. Z. Dr Mark, "Digital System Design with System Verilog", Pearson, 2010.
3. Luciano Lavagno, Igor L. Markov, Grant E. Martin, Louis K. Scheffer, "Electronic Design Automation for Integrated Circuits Handbook, Second Edition", ISBN 9781032339986,2022.

REFERENCE BOOKS

1. Robert Ashby, "Designer's Guide to the Cypress PSoC,Newnes (An imprint of Elsevier)", 2006.
2. S.Sutherland, S. Davidmann and P. Flake, "System Verilog for Design", 2nd Edition, Springer, 2006.
3. M.J.S.Smith, "Application Specific Integrated Circuits",Pearson, 2008.
4. M.H.Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", Pearson, 2004.
5. O.H. Bailey, "The Beginner's Guide to PSoC", Express Timelines Industries Inc,2007.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	1	1
CO2	2	2	1	2	1	1
CO3	2	1	1	2	2	1
CO4	2	1	1	2	2	1

CO5	2	2	2	1	2	1
AVG	2	1	1	2	2	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL2303 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY **L T P C 3 1 0 4**

COURSE OBJECTIVES

- To gain broad conceptual understanding of the various aspects of electromagnetic (EM) interference and compatibility and electromagnetic shielding effectiveness
- To understand ways of mitigating EMI by using shielding, grounding and filtering
- To understand how EMI impacts wireless and broadband technologies

UNIT I INTRODUCTION & SOURCES OF EM INTERFERENCE 12

Introduction - Classification of sources - Natural sources - Man-made sources - Survey of theelectromagnetic environment.

UNIT II EM SHIELDING 12

Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency,magnetic field shielding - Effects of apertures

UNIT III INTERFERENCE CONTROL TECHNIQUES 12

Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing -Signal-line filters - Nonlinear protective devices.

UNIT IV EMC STANDARDS, MEASUREMENTS AND TESTING 12

Need for standards - The international framework - Human exposure limits to EM fields -EMCmeasurement techniques - Measurement tools - Test environments.

UNIT V EMC CONSIDERATIONS IN WIRELESS AND BROADBAND TECHNOLOGIES 12

Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.

Case Study:

1. Investigate various case studies related to EMIC. Example: Chernobyl Disaster in 1986.
2. Develop some understanding about the design of EM shields in electronic system design and packaging.

TOTAL: 60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the student will be able to

CO1: Demonstrate knowledge of the various sources of electromagnetic interference.
CO2: Display an understanding of the effect of how electromagnetic fields.
CO3: Explain the EMI mitigation techniques of shielding and grounding
CO4: Explain the need for standards and EMC measurement methods
CO5: Discuss the impact of EMC on wireless and broadband technologies

TEXTBOOKS

1. Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press,Second Edition, Indian Edition, 2013.
2. Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition,2008.
3. Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010.

REFERENCE BOOKS

1. Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork,2009.
2. Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 1997.
3. Paolo Stefano Crovetti, "Electromagnetic Interference and Compatibility", Electronics,2021.
4. Reto B. Keller, "Design for Electromagnetic Compatibility--In a Nutshell", Springer,2023.
5. L. Ashok Kumar, Y. Uma Maheswari, "Electromagnetic Interference and Electromagnetic Compatibility Principles, Design, Simulation, and Applications", CRC Press,2024.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	1	1
CO2	2	1	1	2	1	1
CO3	2	1	1	2	1	1
CO4	2	1	1	2	1	1
CO5	2	1	1	2	1	1
AVG	2	1	1	2	1	1

1-Low, 2-Medium, 3-High, '-'-No Correlation

24VL2304	DATA CONVERTERS	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES

- To teach Analog to Digital and Digital to Analog Converters characteristics.
- To develop the skills to design of Switched Capacitor based Circuits.
- To train the students to design of Analog to Digital and Digital to Analog Converters.

UNIT I INTRODUCTION & CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS **12**

Evolution, Types and Applications of AD/DA Converter Characteristics, Issues in Sampling, Quantization and Reconstruction, Oversampling and Anti-aliasing Filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS **12**

Switched-Capacitor Amplifiers, Switched Capacitor Integrator, Switched Capacitor Common Mode Feedback. Single Stage Amplifier as Comparator, Cascaded Amplifier Stages as Comparator, Latched Comparators. Offset Cancellation, Op Amp Offset Cancellation, Calibration Techniques.

UNIT III TYPES OF D/A CONVERTERS **12**

Current Steering DACS, Capacitive DACS, Binary Weighted Vs. Thermometer DACS, Issues in Current Element Matching, Clock Feed Through, Zero Order Hold Circuits, DNL, INL and Other Performance Metrics of ADCS and DACS.

UNIT IV PIPELINE AND OTHER ADCS **12**

Performance Metrics, Flash Architecture, Pipelined Architecture, Successive Approximation Architecture, Time Interleaved Architecture.

UNIT V SIGMA DELTA CONVERTERS **12**

First Order and Second Order Sigma Delta Modulator Characteristics.

Case Study:

1. Analyze the architecture, function and application of Analog-Digital converters (A/D) Sigma-Delta showing some simulations using the Simulink software.
2. The use of Artificial Intelligence (AI) to manage the operation and improve the performance of Analog-to-Digital Converters (ADCs) based on Sigma-Delta Modulators.

TOTAL:60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to:

CO1: Analyse the various blocks associated with a typical CMOS AD or DA Converter.
CO2: Design and implement circuits using switched capacitor concepts.
CO3: Analyze and design D/A converters.

CO4: Discuss different types of A/Ds .
CO5: Analyze and design Sigma Delta converter.

TEXT BOOKS

1. Behzad Razavi, "Principles of Data Conversion System Design", IEEE Press,1995.
2. Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog
3. Converters" Kluwer Acedamic Publishers, Boston, 2003.

REFERENCE BOOKS

1. J. G. Proakis, D. G. Manolakis, "Digital Signal Processing Principles, Algorithms and Applications", Prentice Hall, 4th Edition, 2006.
2. Shanthi Pavan, Richard Schreier, Gabor C. Temes , "Understanding Delta-Sigma Data Converters", Willey –IEEE Press, 2nd Edition, 2017.
3. Franco Maloberti, "Data Converters", Springer Science & Business Media, 2007.
4. Walt Kester, Newnes, "The Data Conversion Handbook", Analog-Digital Conversion,2004.
5. Ahmed M. A. Ali, "High Speed Data Converters", ISBN:978-1-84919-938-4,2016.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	1	1
CO2	2	1	1	2	1	1
CO3	2	1	1	2	1	1
CO4	2	1	1	2	1	1
CO5	2	1	1	2	1	1
AVG	2	1	1	2	1	1

1-Low, 2-Medium, 3-High, '-'- No Correlation

24VL2305 HARDWARE SOFTWARE CO-DESIGN FOR FPGA **L T P C**
3 1 0 4

COURSE OBJECTIVES

- To acquire the knowledge about system specification and modelling
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING **12**

Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor Architectures with Many ASICs.

UNIT II HARDWARE/SOFTWARE PARTITIONING **12**

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS **12**

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION **12**

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure.

UNIT V DESIGN SPECIFICATION AND VERIFICATION **12**

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification.

Case Study:

1.HW/SW Partitioning Based On Heuristic Scheduling and Genetic Algorithms.

2.Illustrate the design flow using single-chip codesign of an Internet video game.

TOTAL:60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Describe The Broad Range of System Architectures and Design Methodologies.
CO2: Discuss the Data flow Models as a State-of-the-Art Methodology.
CO3: Understand in Translating between Software and Hardware descriptions.
CO4: Understand the State-of-The-Art practices in developing Co-Design Solutions.
CO5: Understand the Concurrent Specification from an Algorithms.

TEXT BOOKS

1. Patrick Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer,2010.
2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Publisher, 1998.
3. J. H. Reed, Software Radio, Pearson, 2002.

REFERENCE BOOKS

1. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Publisher,1997.
2. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design”, Kaufmann Publisher,2001.

3. Tsui, Digital Techniques for Wideband receivers, Artech House, 2001.
4. S. K. Mitra, Digital Signal processing, McGrawHill, 1998.
5. U. Meyer – Baese, Digital Signal Processing with FPGAs, Springer, 2004.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	1	1
CO2	2	1	1	2	1	1
CO3	2	1	1	2	1	1
CO4	2	1	1	2	1	1
CO5	2	1	1	2	1	1
AVG	2	1	1	2	1	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL2306 SCRIPTING LANGUAGES FOR ELECTRONIC DESIGN AUTOMATION **L T P C 3 1 0 4**

COURSE OBJECTIVES

- To write scripts in the LINUX environment.
- To study the principles of Scripting Languages like Perl,TCL and Python.
- To write the scripts for automation using the languages like Perl,TCL and Python.

UNIT I LINUX BASICS **12**

Introduction to Linux,File System of Linux,General usuage of Linux Kernel and Basic Commands,Linux users and group,Permissions for File,directory and users,Searching a file and directory,zipping and unzipping concepts.

UNIT II PERL BASICS **12**

History and concepts of PERL,Scalar data,Arrays and List Data,Control Structures,Hashes,Basics I/O,Regular Expressions,Functions,Miscellaneous Control Structures,Formats.

UNIT III TCL BASICS **12**

An overview of TCL and Tk,TCL Language syntax,Variables,Expressions,Lists,Control flow,procedures,Errors and Exceptions,String manipulations.

UNIT IV ADVANCED TOPICS IN PERL **12**

Directory Acesses,File and Directory Manipulation,Process Manipulation,Packages and Modules,Applications of PERL Scripts to Electronic Design Automation.

UNIT V ADVANCED TOPICS IN TCL **12**

Acessing Files and Processes.

Case Study:

1. A Case Study on TCL Language.
2. To study more features of TCL to identify if they strengthen or weaker original design principles.

TOTAL:60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Explain and apply commands in LINUX Environment.
CO2: To develop and execute PERL scripts.
CO3: To analyze and handle files, directories and manage process using PERL.
CO4: Build TCL scripts to handle files, directories and manage process.
CO5: To develop Python scripts to interpret files and directories.

TEXT BOOKS

1. Guido van Rossum Fred L.Drake,Jr.,editor,Python Tutorial Release 3.2.3,2012,Python Software Foundation.
2. Henry Frankland, "Linux RHEL 6 and above; windows 10", EDA solutions ,2021.
3. Laung-Terng Wang, Yao-Wen Chang and Kwang-Ting (Tim) Cheng, "Electronic Design Automation",Science direct,2009

REFERENCE BOOKS

1. Mark Lutz,Learning Python,2013,5th Edition,O'Reilly Media,Inc
2. Suman Lata Tripathi, Abhishek Kumar, Jyotirmoy Pathak , "Programming and GUI Fundamentals: TCL-TK for Electronic Design Automation (EDA)", Wiley,2022.
3. Kirti Sikri Desai, "EDA tools and Programming Languages, and Tcl", 1945.
4. Konrad Zuse, "first high-level programming language",1942.
5. Corrado Böhm, "first high-level language to have an associated compiler", 1951.

Mapping of COs and POs

COs	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	1	2	1	1
CO2	2	1	1	2	1	1
CO3	2	1	1	2	1	1
CO4	2	1	1	2	1	1
CO5	2	1	1	2	1	1
AVG	2	1	1	2	1	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL2102 LOW POWER VLSI DESIGN L T P C
3 1 0 4

COURSE OBJECTIVES

- To provide a comprehensive idea about different sources of power dissipation in VLSI circuits.
- To introduce power estimation methods, understand different power optimization methods and challenges.
- To design a system with multiple supply and threshold voltages applicable for various applications.

UNIT I VARIOUS SOURCES OF POWER DISSIPATION 12

Importance of Low Power Consumption – Design for Low Power – Deep Submicron and Nanometer MOS Transistors and Models – Sources of Static and Dynamic Power Consumption in MOS Devices New Device Technologies for Reducing Leakage Current – Basics of Power and Energy.

UNIT II ESTIMATE THE POWER OF GIVEN CIRCUIT 12

Power Optimization during Design Cycle – Architecture – Algorithm and System Levels – Power Optimization of Interconnects and Clocks – Dynamic Voltage Scaling – Clock Distribution – RTL power estimation and optimization – Model granularity – Model parameters – Model semantics – Model storage and Model construction.

UNIT III DESIGN OF LOW POWER DIGITAL VLSI CIRCUIT 12

Power Optimization in Memories – Power in Cell Arrays – Power for Read and Write Accesses – Low Power Memory Technologies – Standby Power Optimization of Circuits and Systems – Power Optimization of Circuits and Systems during Operation – Low Power Design Methodologies and Flows Power Characterization and Modeling – Low Power Clock – Data and Power Gating – Power Integrity.

UNIT IV LEAKAGE POWER REDUCTION 12

Leakage power reduction technique- stacking technique, sleepy keeper technique, super cutoff CMOS,VTCMOS, MTCMOS, DTCMOS, - energy constrained and delay constrained. Sleep Transistor design Switch efficiency, area efficiency, IR drop, normal Vs reverse body bias, Inrush current and current Latency, Power gating – course grain and fine grain. Isolation, retention, power down and wake up methods.

UNIT V CASE STUDY- LOW POWER TECHNIQUE AUTOMATION 12

Low power design techniques automation levels, Power-Aware design flow, Unified power format (UPF): Necessity, UPF Tutorial, Case study:Low power design examples using UPF, Design flow modification with UPF.

TOTAL:60 PERIODS

COURSE OUTCOMES

On successful completion of this course, students will be able to

CO1: Understanding about various sources of power dissipation.

CO2: Estimate the power for given circuits.

CO3: Design low power digital VLSI circuits.

CO4: Apply various circuit techniques to optimize the power consumption.

CO5: Analyze and explore the usage of sleep transistors and IP Design for low power.

TEXT BOOKS

1. Jan M. Rabaey, Low Power Design Essentials, Springer, 2009. Christian Piguet, Low-Power CMOS Circuits: Technology, Logic Design a, CRC Press, Taylor and Francis, 2006.
2. RakeshChadha and J. Bhaskar, An ASIC Low Power Primer, Analysis, Techniques and Specification, Springer,2013.
3. Ajit Pal, "Low-Power VLSI Circuits and Systems", Springer 2015.

REFERENCE BOOKS

1. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi,2006.
2. Methodology Manualfor System on Chip,Springer, 2007.
3. Gary K. Yeap, Farid N. Najm, "Low Power Vlsi Design and Technology", World Scientific, 1996.
4. Shilpi Birla, Shashi Kant Dargar, Neha Singh, P. Sivakumar, "Low Power Designs in Nanodevices and Circuits for Emerging Applications", ISBN 9781032412771,2014.
5. Abdellatif Bellaouar,Mohamed I. Elmasry University of Waterloo, "Low-Power Digital Vlsi Design Circuits and Systems",Springer,1995.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	1	2	2	1
CO2	2	1	1	2	2	1
CO3	2	1	1	2	2	1
CO4	2	1	1	2	2	1
CO5	2	1	1	2	2	1
AVG	2	1	1	2	2	1

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL3301 **MEMS AND NEMS** **L T P C**
3 1 0 4

COURSE OBJECTIVES

- To introduce the concepts of Micro Electro Mechanical devices and fabrication process of microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of Quantum Mechanics and Nano systems.

UNIT I OVERVIEW **12**

New trends in Engineering and Science: Micro and Nanoscale systems, introduction to design of MEMS and NEMS, MEMS and NEMS – applications, devices and structures. Materials for MEMS: Silicon, Silicon compounds, polymers, metals

UNIT II MEMS FABRICATION TECHNOLOGIES **12**

Microsystem Fabrication Processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin Film Depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching Techniques: Dry and Wet Etching, Electrochemical Etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-Like) Technology; Packaging: Microsystems Packaging, Essential Packaging Technologies, Selection of Packaging Materials

UNIT III MICRO SENSORS **12**

MEMS Sensors: Design of Acoustic Wave Sensors, Resonant Sensor, Vibratory Gyroscope, Capacitive and Piezo Resistive Pressure Sensors- Engineering Mechanics Behind These Microsensors. Case Study: Piezo-Resistive Pressure Sensor.

UNIT IV MICRO ACTUATORS **12**

Design of Actuators: Actuation Using Thermal Forces, Actuation Using Shape Memory Alloys, Actuation Using Piezoelectric Crystals, Actuation using Electrostatic Forces (Parallel Plate, Torsion Bar, Comb Drive Actuators), Micromechanical Motors and Pumps. Case Study: Comb Drive Actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS **12**

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave Function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their Quantization, Molecular Wires and Molecular Circuits

TOTAL: 60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the student will be able to

CO1: Discuss micro sensors
CO2: Explain micro actuators
CO3: Outline nanosystems and Quantum mechanics
CO4: Design micro actuators for different applications
CO5: Analyze atomic structures

TEXT BOOKS

1. Chang Liu, "Foundations of MEMS", Pearson Education India Limited, 2006.
2. Marc Madou, "Fundamentals of Microfabrication", CRC Press 1997.
3. Stephen D. Senturia," Micro System Design", Kluwer Academic Publishers,2001

REFERENCE BOOKS

1. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.
2. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata Mcraw Hill, 2002.
3. Deilang chan, "Nems/Mems technology devices", Scientific.Net,2011.
4. Cornelius T. Leondes, "Mems and Nems handbook techmolgies and applications", Springer,2006.
5. Zhuoqing Yang, "Advanced MEMS/NEMS Fabrication and Sensors", Springer,2022.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	2	1	-	-
CO2	1	-	2	1	-	-
CO3	1	-	2	1	-	-
CO4	1	-	2	1	2	-
CO5	1	-	2	1	-	-
AVG	1	-	2	1	2	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL3302 NETWORK ON CHIP L T P C
3 1 0 4

COURSE OBJECTIVES

- Understand the concept of Network - on - Chip
- Learn router architecture designs
- Study fault tolerance Network - on – Chip

UNIT I INTRODUCTION TO NOC 12

Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality- of-Service Support

UNIT II ARCHITECTURE DESIGN **12**

Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design

UNIT III ROUTING ALGORITHM **12**

Packet Routing-QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable andAdaptive Routing Algorithms

UNIT IV TEST AND FAULT TOLERANCE OF NOC **12**

Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance For Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP **12**

Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation For QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling For Networks-On-Chip

TOTAL:60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students will be able to

CO1: Compare different architecture design
CO2: Discuss different routing algorithms
CO3: Explain three dimensional Networks on Chip architectures
CO4: Test and design fault tolerant NOC
CO5: Design three dimensional architectures of NOC

TEXT BOOKS

1. Chrysosto MOSnicopoulos, Vijaykrishnan Narayanan, Chita R.Das “Networks-On - Chip Architectures Holistic Design Exploration”, Springer.
2. Fayezgebali, Haythamelmiligi, Hqhahedwatheq E1-Kharashi “Networks-On-Chips Theory and Practice CRC Press.
3. Kundu, Santanu, Chattopadhyay, Santanu, “Network-on-Chip”, Taylor & Francis,2014.

REFERENCES BOOKS

1. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On- Chip Architectures” 2013.
2. Palesi, Maurizio, Masoud “Routing Algorithms in Networks-On-Chip” 2014.
3. Natalie Enright Jerger , Li-Shiuan Peh, “On-Chip Networks”, Springer,2009.
4. Fayez Gebali, “Networks-on-Chips: Theory and Practice”, CRC Press, 2011.

5. Subodha Charles, "Design Of Secure And Trustworthy Network-On-Chip Architectures", University Of Florida,2020

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	1	1	-	-
CO2	1	-	1	1	-	-
CO3	1	-	1	1	-	-
CO4	1	-	1	1	-	-
CO5	1	-	1	1	-	-
AVG	1	-	1	1	-	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL3303 NANO TECHNOLOGY L T P C

3 1 0 4

COURSE OBJECTIVES

- Provides knowledge of various industrial applications of Nanotechnology.
- Imparting the state of art of nanotechnology to the society and to the environmental implication.
- To exercise the students' knowledge and imagination of Nanoscience and nanotechnology toward engineering applications coupled with detailed justifications.

UNIT I NANOTECHNOLOGY 12

Background, what is Nanotechnology, types of Nanotechnology and Nano-machines, top down and bottom up techniques, atomic manipulation-Nanodots, semi-conductor quantum dots, self- assembly monolayers, simple details of characterization tools- SEM, TEM, STM, AFM.

UNIT II NANOMATERIALS 12

Nanomaterials, Preparation of Nanomaterials- solid state reaction method, Chemical Vapor Deposition, SOL-GELS techniques, electrodeposition, ball milling, introduction to lithography, Pulse Laser Deposition (PLD), applications of Nanomaterials

UNIT III CARBON TUBES 12

New forms of carbon, carbon tubes-types of Nanotubes, formation of Nanotubes, assemblies, purification of carbon Nanotubes, properties of Nanotubes, applications of Nanotubes

UNIT IV OPTICS, PHOTONICS AND SOLAR ENERGY 12

Light and Nanotechnology, interaction of light and Nanotechnology, Nanoholes and photons, solarcells, optically useful Nanostructured polymers, photonic crystals.

UNIT V FUTURE APPLICATIONS **12**

MEMS, Nanomachines, Nanodevices, Quantum Computers, Opto-electronic Devices, Quantum Electronic devices, environmental and biological applications.

TOTAL: 60 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students should will be able to:

CO1: Understand the bases for introduction to Nanotechnology
CO2: Understand the synthesis of Nanomaterials and their application and the impacts.
CO3: Acquire knowledge about various kind of Nano materials
CO4: Understand the Nanotechnology devices used and their structures
CO5: Understand and improve the application of Nanotechnology

TEXT BOOKS

1. Mick Wilson, Kamali Kannangra Geoff Smith, Michelle Simons and Burkhard Raguse,"Nanotechnology-Basic Science and Emerging Technologies", Overseas Press, 2002
2. Mark Ratner and Daniel Ratner, "Nanotechnology-a Gentle Introduction to The Next Big Idea",Prentice Hall,2003
3. Bhushan, ""Handbook of Nanotechnology", Springer,2017

REFERENCE BOOKS

1. Rebecca L Johnson,"Nanotechnology", Lerner Publications,2003.
2. Charles P. Poole Jr., "Introduction to Nanotechnogy", Chapman and Hall/CRS, 2003.
3. Jeremy.J.Remsdon, "Nanotechnology An Introduction", Pearson,2010.
4. Goodard William A, Donald W Brenner, "Handbook of Nanoscience, Engineering, and Technology", CRC Press,2007
5. Yasir Waheed ,"Core Concept of Nanotechnology with application spectrum", Spectram books,2007.

Mapping of COs and POs

COs	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	1	1	-	-
CO2	1	-	1	1	-	-
CO3	1	-	1	1	-	-
CO4	1	-	1	1	-	-
CO5	1	-	1	1	-	-
AVG	1	-	1	1	-	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL3304 **EVOLVABLE HARDWARE** **L T P C**
3 0 0 3

COURSE OBJECTIVES

- To study about the evolvable systems algorithms, multi-objective utility functions
- Understand the concepts of reliability, design-in redundancy, fault tolerance and defect tolerance
- Design of evolvable systems using Programmable Logic Devices (like FPGAs) and modular subsystems with identical components and generalized controller algorithms

UNIT I INTRODUCTION **9**

Traditional Hardware Systems and its Limitations, Evolvable Hardware, Characteristics of Evolvable Circuits and Systems, Technology-Extrinsic and Intrinsic Evolution offline and Online Evolution, Applications and Scope of EHW

UNIT II EVOLUTIONARY COMPUTATION **9**

Fundamentals of evolutionary algorithms, components of EA, variants of EA, Genetic Algorithms, genetic programming, evolutionary strategies, evolutionary programming, implementations – evolutionary design and optimizations, EHW – current problems and potential solutions

UNIT III RECONFIGURABLE DIGITAL DEVICES **9**

Basic architectures – Programmable Logic Devices, Field Programmable Gate Arrays (FPGAS), using reconfigurable hardware – design phase, execution phase, evolution of digital circuits

UNIT IV RECONFIGURABLE ANALOG DEVICES **9**

Basic architectures – Field Programmable Transistor Arrays (FPTAS), analog arrays, MWMS,using reconfigurable hardware – design phase, execution phase, evolution of analog circuits

UNIT V PPLICATIONS OF EHW **9**

Synthesis vs. Adaptation, designing self-adaptive systems, fault-tolerant systems, real-time systems, intrinsic reconfiguration for online systems, EHW based fault recovery and future work

TOTAL:45 PERIODS

COURSE OUTCOMES

On successful completion of this course, the students should will be able to

CO1: Understand the fundamentals of computational models and computers.

CO2: Understand the principles of bio-inspired and unconventional computational systems.

CO3: Discuss about the reconfigurable digital architectures and its computational intelligence techniques.

CO4: Discuss about the reconfigurable analog architectures and its computational intelligence techniques.

CO5: Discuss about the typical applications of bio-inspired and other unconventional techniques in the phase of design, implementation and runtime of a computational device.

TEXT BOOKS

1. Garrison W. Greenwood and Andrew M. Tyhrrell, "Introduction to Evolvable Hardware: a Practical Guide for Designing Self- Adaptive Systems", Wiley-Ieee Press, 2006.
2. Tetsuya Higuchi, Xin Yao and Yong Liu, "Evolvable Hardware", Springer-Verlag, 2004.
3. David R. W. Smith, "Evolvable Hardware: From Theory to Practice",Springer,2010.

REFERENCE BOOKS

1. Lukas Sekanina, "Evolvable Components: From Theory to Hardware Implementations", Springer, 2004.
2. Timothy G. W. Gordon, " Evolving Hardware", Springer 2005.
3. Martin A. Trefzer , Andy M. Tyrrell, "Evolvable Hardware from Practice to Application", Springer 2015.
4. Tetsuya Higuchi, Yong Liu, Xin Yao, "Evolvable Hardware", Spinger,2006.
5. André Macário Barros, Heitor Silvério Lopes, "Encyclopedia of Information Science and Technology, Third Edition", IGI Global,2015.

Mapping of COs and POs

COs	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	-	1	1	-	-
CO2	1	-	1	1	-	-
CO3	1	-	1	1	-	-
CO4	1	-	1	1	-	-
CO5	1	-	1	1	-	-
AVG	1	-	1	1	-	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL3305 SOFT COMPUTING AND OPTIMIZATION TECHNIQUES L T P C
3 0 0 3

COURSE OBJECTIVES

- To classify various soft computing frame works.
- To be familiar with the design of neural networks, fuzzy logic, and fuzzy systems.
- To learn mathematical background for optimized genetic programming and be exposed to neuro-fuzzy hybrid systems and its applications.

UNIT I FUZZY LOGIC 9

Introduction to Fuzzy logic - Fuzzy sets and membership functions- Operations on Fuzzy sets- Fuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzylogic controller design- Some applications of Fuzzy logic.

UNIT II ARTIFICIAL NEURAL NETWORKS 9

Supervised Learning: Introduction and how brain works, Neuron as a simple computing element, The perceptron, Backpropagation networks: architecture, multilayer perceptron, backpropagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network. Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self- Organizing Computational Maps: Kohonen Network.

UNIT III GENETIC ALGORITHM 9

Genetic algorithm- Introduction - biological background - traditional optimization and search techniques - Genetic basic concepts - operators – Encoding scheme – Fitness evaluation – crossover - mutation - Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

UNIT IV NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems (ANFIS) – architecture - Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – the inverted pendulum system.

UNIT V CONVENTIONAL OPTIMIZATION TECHNIQUES 9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient- conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

TOTAL :45 PERIODS

COURSE OUTCOMES

On successive completion of this course, the students will be able to

CO1: Develop application on different soft computing techniques.

CO2: Implement Neuro-Fuzzy and Neuro-Fuzz-GA expert system.

CO3: Implement machine learning through Neural networks.
CO4: Model Neuro Fuzzy system for clustering and classification.
CO5: Able to use the optimization techniques to solve the real world problems

TEXT BOOKS

1. J.S.R.Jang, C.T. Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI / Pearson Education 2004.

2. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
3. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications, Prentice Hall, 1995.

REFERENCE BOOKS

1. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.
2. Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.
3. Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.
4. James A. Freeman , Neural Networks Algorithms, Applications, Pearson Edn., 2003.
5. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.

Mapping of COs and POs

COs	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	-	2	1	2	-
CO2	1	-	2	1	2	-
CO3	1	-	2	1	2	-
CO4	1	-	2	1	2	-
CO5	1	-	2	1	-	-
AVG	1	-	2	1	2	-

1-Low, 2-Medium, 3-High, '-'- No correlation

24VL3306 CAD FOR VLSI DESIGN L T P C
3 0 2 4

COURSE OBJECTIVES

- To introduce the VLSI design methodologies, data structures and algorithms required for VLSI design.
- To study algorithms for partitioning, placement, floor planning and routing.
- To study algorithms for modelling, simulation and synthesis.

UNIT I INTRODUCTION **9**

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Reviewof VLSI Design Automation Tools

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS **9**

Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

UNIT III ALGORITHMS FOR PARTITIONING AND PLACEMENT **9**

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction –Partitioning – Placement – Placement Algorithms.

UNIT IV ALGORITHMS FOR FLOORPLANNING AND ROUTIN **9**

Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing –Global Routing – Detailed Routing.

UNIT V MODELLING, SIMULATION AND SYNTHESIS **9**

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.

TOTAL:45 PERIODS

COURSE OUTCOMES

On successive completion of this course, the students should be able to

CO1: Use various VLSI design methodologies
CO2: Understand different data structures and algorithms required for VLSI design.
CO3: Develop algorithms for partitioning and placement.
CO4: Develop algorithms for floor planning and routing.
CO5: Design algorithms for modelling, simulation and synthesis.

TEXT BOOKS

1. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India, 2017.
2. Naveed a. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, Springer, 2017.
3. R.H. Katz, “Contemporary logic design”, Addison-Wesley Pub. Co., 1993.

REFERENCE BOOKS

1. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition,
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
3. Ramachandran, “Digital VLSI systems design”, Springer, 2007.

4. M. Sarrafzadeh and C.K. Wong, An introduction to physical design, McGraw Hill, 1996.
5. J. Bhasker, Verilog VHDL synthesis: a practical primer, B S Publications, 1998.

Mapping of COs and POs

COs	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	0	1	2	-	-
CO2	1	0	1	2	-	-
CO3	1	0	1	2	2	-
CO4	1	0	1	2	2	1
CO5	1	0	1	2	2	1
AVG	1	0	1	2	2	1

1-Low, 2-Medium, 3-High, '-'- No correlation

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